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4. Mechanical Characteristics Data

TFT Model	ITSV50D1
Physical Size	278mm x 200mm x 6.8mm(Typ.)
Screen Diagonal	30.8cm(12.1")
Active Area	246.0mm(H) x 184.5mm(V)
Pixel Format	800(x3) x 600
Pixel Pitch	0.3075(per one triad) x 0.3075 mm
Pixel Arrangement	R,G,B Vertical Stripe
Weight	450 grams Typ.
LCD Surface Treatment	Antiglare and Hard coat 3H
Backlight	Single cold-cathode fluorescent lamp

5. Absolute Maximum Ratings

Electrical Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD	-0.3 to +6.0	V	
Lamp ignition voltage	V _{cd}	1500	V _{rms}	At 0 degreeC
Input Voltage	V _{IN}	-0.3 to +5.25	V	
CFL Discharge Current	I _{cd}	5	mA _{rms}	Exclude inrush current
CFL Inrush Current	I _{Rcd}	30	mA _{0-p}	With Max. duration = 50 (mSec)
CFL Driving Frequency	f _{CFL}	30 to 70	kHz	At 25 degreeC
Static Electricity				Operators should be grounded in handling the TFT LCD Module

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5. Absolute Maximum Ratings (continued)

Environmental Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Storage Temperature	TST	-20 to +60	degC	At the glass surface
Operation Temperature	TOP	0 to +50	degC	At the glass surface
Operation Humidity		5 to 80	%RH	Max wet bulb temp. 29 degC No condensation
Vibration		1.5	G	10 to 200 Hz, X,Y,Z (Note 1)
Trapezoidal Shock		50	G	18 msec, +/- X,Y,Z (Note 1)
Half-sine Shock		210	G	3 msec, +/- X,Y,Z (Note 1)
Corrosive Gas		Not Acceptable		

Note 1 : At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture..

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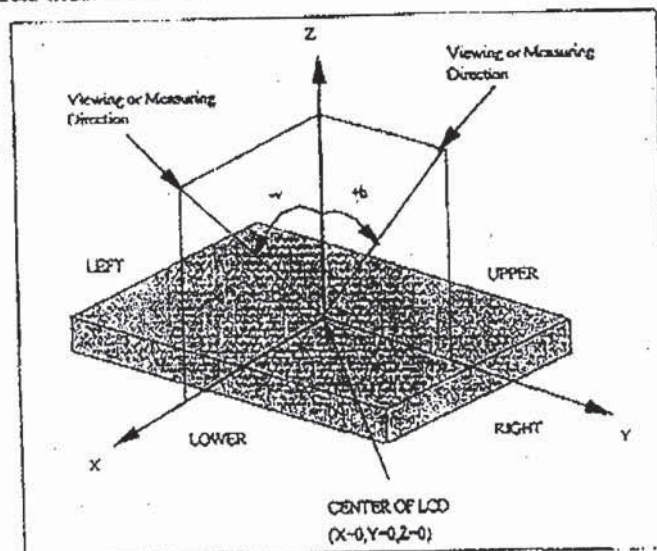
6. Optical Characteristics

Item	Conditions	Specification			Unit	Notes
		Min.	Typ.	Max.		
Viewing Angle	$h = 0, v = +20$	5				In the unit of Contrast Ratio K
	$h = 0, v = -20$	20				
	$h = \pm 40, v = 0$	10				
	$h = \pm 20, v = 0$	45				
Contrast	$h = 0, v = 0$	60	100			In the unit of Contrast Ratio K
Response Time	Both On/Off From/To 10% luminance To/From 90% luminance level.		30	50	msec	Ambient Temperature 25degC. At Center of LCD. $h = 0, v = 0$
White Luminance	Gray Scale L= L63 $h = 0, v = 0$. CFL Power Consumption = 1.5W	57	70		cd/m ²	At Center of LCD
Luminance Uniformity	Adjacent Area	0.80				Ratio of (Ldark / Lbright) over a circular area of 10 mm diameter placed anywhere on the screen.
	Screen Total	0.59				Ratio of (Ldark / Lbright) over the entire screen
Chromaticity	Red x		0.540			+/- 0.040
	Red y		0.333			+/- 0.030
	Green x		0.312			+/- 0.030
	Green y		0.546			+/- 0.030
	Blue x		0.162			+/- 0.030
	Blue y		0.161			+/- 0.040
White Balance	x		0.312			+/- 0.030
	y		0.360			+/- 0.030

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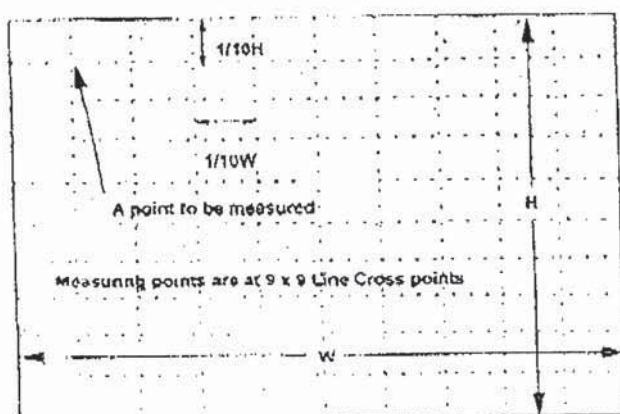
Notes for the Optical Characteristics :



- Gray Scale Level is denoted by L_{xx} . (ex. L_{00} means all Pels are in the selected state) .

(Uniformity Measurement)

- 'Lbright' represents the Luminance of the point that is brighter than the other point to be compared
- 'Ldark' represents the Luminance of the point that is darker than the other point to be compared
- Measuring points are shown in the following Fig.



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8. Quality Specifications

8.1 General Criteria of TFT-LCD Quality Specification

8.1.1 External Inspection Quality

Table 1 describes the external inspection quality of the general TFT-LCD module at power-off.

Table 1. Specification of External Inspection Quality			
Items	Specification		
Polarizer Scratch/Bubble			
Elliptical Scratches/Bubbles	Average Diameter(D)		Counts(N)
	$0.0 < D \leq 0.3 \text{ mm}$ $0.3 < D \leq 0.5 \text{ mm}$ $0.5 < D \text{ mm}$		Disregarded $N \leq 3$ $N = 0$
Linear Scratches/Bubbles	Width(W mm)	Length(L)	Counts(N)
	$0.00 < W \leq 0.07 \text{ mm}$ $0.07 < W \leq 0.1 \text{ mm}$ $0.1 < W \text{ mm}$	$L \leq 5 \text{ mm}$	Disregarded $N \leq 3$ $N = 0$
Bezel Appearance			
Bezel Appearance		Any visible rust shall not be found. Deep damage caused rust shall not be found.	

8.1.2 Line Defect

No visible line defect is allowed in entire screen.

A Line Defect is defined as a horizontal and vertical apparent line, visible through 5% ND-filter, that differs from adjacent lines at any gray raster pattern.

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8.2 Unique Specification of SVGA TFT-LCD Display

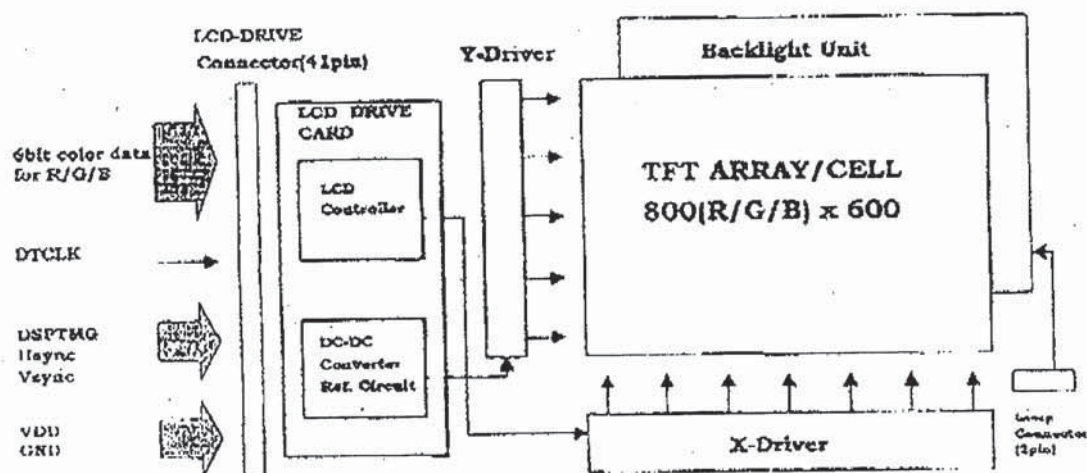
This Quality Specification is for the SVGA TFT-LCD module ITSV50D supplied from IBM Corporation to the customers.

8.2.1 Bright and Black Dots

Table 2 describes the specification of bright and black dots in the visual screen quality of the TFT-LCD module at power-ON.

Table 2. Specification of Bright and Black Dots for SVGA TFT-LCD modules	
Items	Specification
Bright Dots	5 Max
Black Dots	5 Max
Bright and Black Dots(total)	8 Max
Two Joined Bright Dots / Two Joined Black Dots	0
Two Joined Dots of Bright and Black Combination	2 Max
Bright/Black Dots Distance (Any Combination)	10 mm Min
Definitions:	
1. A Bright Dot is any one of a stuck Red, Green or Blue pixel visible through 5% ND-filter under all black background.	
2. A Black Dot is a unit pixel under any of red, green or blue bright raster.	
Basic Conditions:	
Viewing Distance:	350 to 500 mm
Ambient Illumination	300 to 700 lux
Ambient Temperature	20 to 25 degreeC

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10. Signal Interface

		Supplier Name	Supplier's Part Number
LCD Drive Connector		HIROSE	DF98-41P-1V
Corresponding Connector		HIROSE	DF98-41S-1V
Pin No.	Signal Name	Description	
15	+RED5	Red Data 5	(MSB)
14	+RED4	Red Data 4	
13	+RED3	Red Data 3	
11	+RED2	Red Data 2	
10	+RED1	Red Data 1	
9	+RED0	Red Data 0	(LSB)
		Red-Pixel-Data	Each red pixel's data consists of these 6 bits pixel data
25	+GREEN5	Green Data 5	(MSB)
24	+GREEN4	Green Data 4	
23	+GREEN3	Green Data 3	
21	+GREEN2	Green Data 2	
20	+GREEN1	Green Data 1	
19	+GREEN0	Green Data 0	(LSB)
		Green-Pixel-Data	Each green pixel's data consists of these 6 bits pixel data
35	+BLUE5	Blue Data 5	(MSB)
34	+BLUE4	Blue Data 4	
33	+BLUE3	Blue Data 3	
31	+BLUE2	Blue Data 2	
30	+BLUE1	Blue Data 1	
29	+BLUE0	Blue Data 0	(LSB)
		Blue-Pixel-Data	Each blue pixel's data consists of these 6 bits pixel data

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2	-DTCLK	Data Clock	The typical frequency is 40.00MHz. The signal is used to strobe the pixel data and +DSPTMG signals. All pixel data shall be valid at the falling edge when the +DSPTMG signal is high.
37	+DSPTMG	Display Timing	This signal strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
5	VSNC	Vertical Sync	The signal is synchronized to -DTCLK.
4	HSNC	Horizontal Sync	The signal is synchronized to -DTCLK.
39,40	VDD	+3.3V	
1,3,6,7,8,12,16,17 18,22,26,27,28,32 36	GND	Signal Ground	
38		Reserved	No connection (Signal reserved)
41		Reserved	No connection (Signal reserved for test)

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

11. Signal Specification

R/G/B, DTCLK, DSPTMG, & VSNC signal specification				
Parameter	Condition	Min.	Max.	Unit
Vih	High level input voltage	2.0	5.0	V
Vil	Low level input voltage	0	0.8	V
Iih	High level input current	---	50	uA
Iil	Low level input current	---	-50	uA

12. Signal Interface for Lamp

		Supplier Name	Supplier's Part Number
Lamp Connector		JST	HR-03VS-1
Pin No.	Signal Name	Description	
1	Lamp High		
3	Lamp Low		

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13. Lamp Interface Specification and Guide Line for CFL Inverter

Parameter Name	Symbol	Min.	Typ.	Max.	Unit	Note
CFL Kick-off Voltage	V_s	-	-	1,100	[V _{RMS}]	$T_{amb}=25\text{ degC}^*$
		-	-	1,500		$T_{amb}=0\text{ degC}^*$
CFL Discharge Current	I_{CFL}	1.5 [†]	-	5.0	[mA _{RMS}]	Total operating range
		-	2.3	-		Screen 70 [cd/m ²], $T_{amb}=25\text{ degC}$
CFL Discharge Voltage	V_{CFL}	-	650	-	[V _{RMS}]	Screen 70 [cd/m ²], $T_{amb}=25\text{ degC}$
CFL Power Consumption	P_{CFL}	-	1.5	-	[W]	Screen 70 [cd/m ²], $T_{amb}=25\text{ degC}$
CFL Discharge Frequency	F_{CFL}	30	40	70 [‡]	[kHz]	Reference [‡]

Note

- *1 All of characteristics listed are measured under the condition using the IBM optional inverter (IBM P/N 46H3650).
- *2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- *3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
- *4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- *5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
- *6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

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14. Interface Timing

Basically, interface timings should match the VESA, 800 x 600 60Hz manufacturing guideline timing.

Symbol	Signal Description	MIN	TYP	MAX	UNIT
f_{clk}	DTCLK frequency	36.00	40.00	40.20	MHz
t_{clk}	DTCLK cycle time	24.88	25.00	27.77	nsec
t_{cll}	DTCLK low width	5.00			nsec
t_{clh}	DTCLK high width	5.00			nsec
t_{clr}	DTCLK rise time			3.00	nsec
t_{clf}	DTCLK fall time			3.00	nsec
t_{dsu}	Data set up time	5.00			nsec
t_{dsh}	Data hold time	5.00			nsec
t_{dsr}	DSPTMG rise time			5.00	nsec
t_{dsf}	DSPTMG fall time			5.00	nsec
t_{dsu}	DSPTMG set up time	5.00			nsec
t_{dsh}	DSPTMG hold time	5.00			nsec
t_x	X total time	848	1056	1088	t_{dx}
t_{ax}	X active time		800		t_{ax}
t_{bx}	X blank time	48	256		t_{bx}
H_{fp}	H-sync front porch	8	40		t_{dx}
H_{bp}	H-sync back porch	8	88		t_{dx}
H_{sync}	H-sync frequency	35.16	37.88	38.46	kHz
H_s	H sync width	8	128		t_{dx}
t_y	Y total time	611	628	1013	t_y
t_{ay}	Y active time		600		t_y
t_{by}	Y blank time		28		t_y
V_{fr}	Frame rate	56.25	60.00	61.00	Hz
V_w	V-sync width	1	4	7	t_y
V_{fp}	V sync front porch	1	1		t_y
V_{bp}	V-sync back porch	9	23	29	t_y

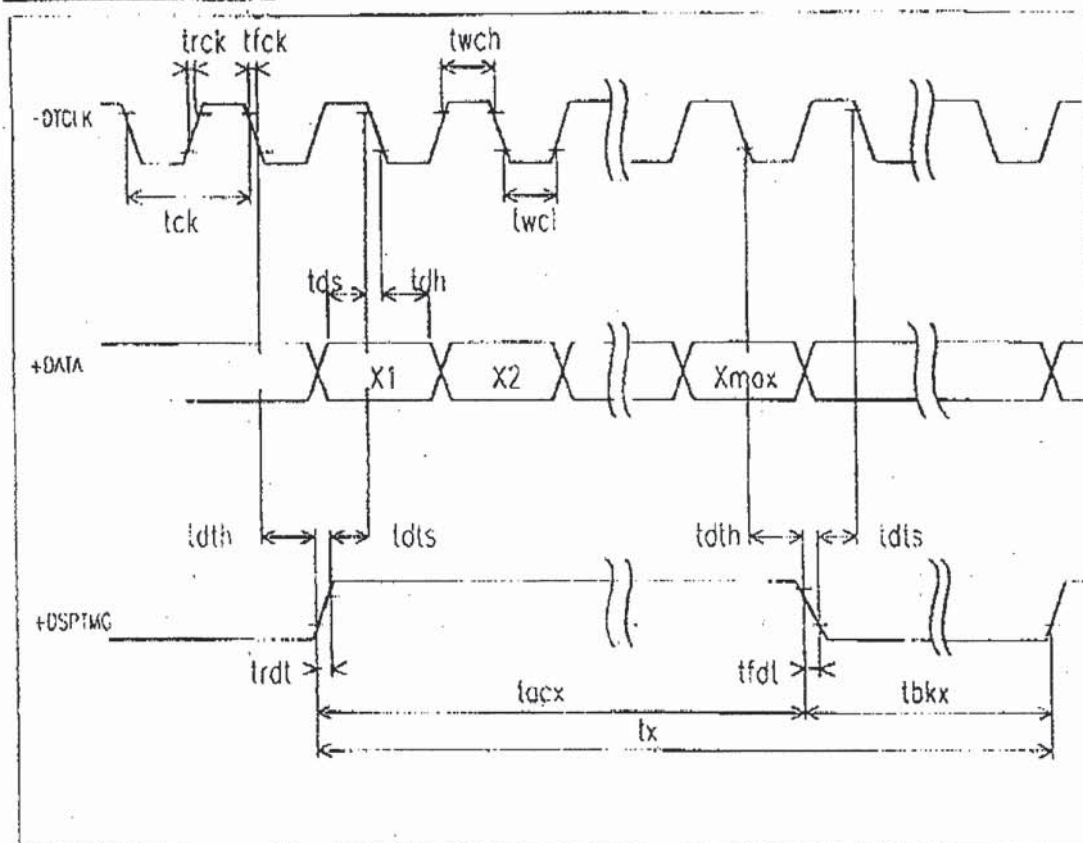
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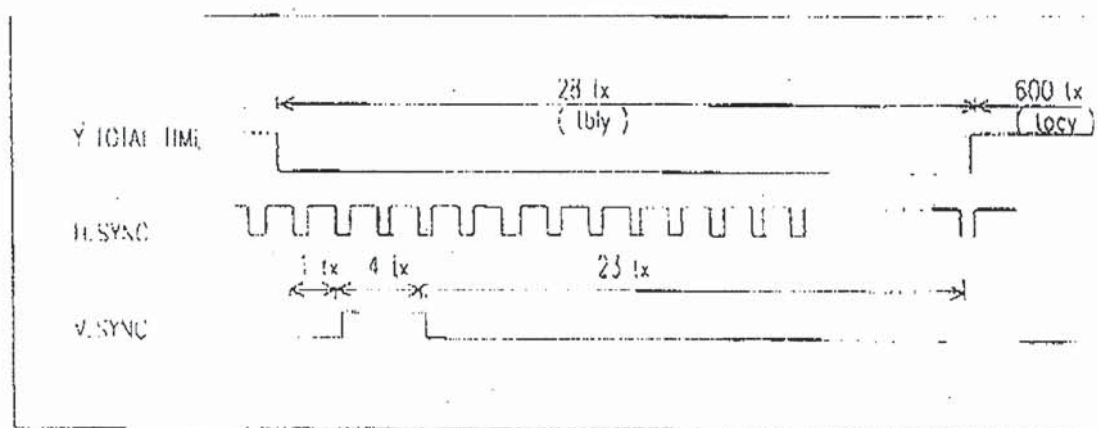
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15. Horizontal Timing



16. Vertical Timing



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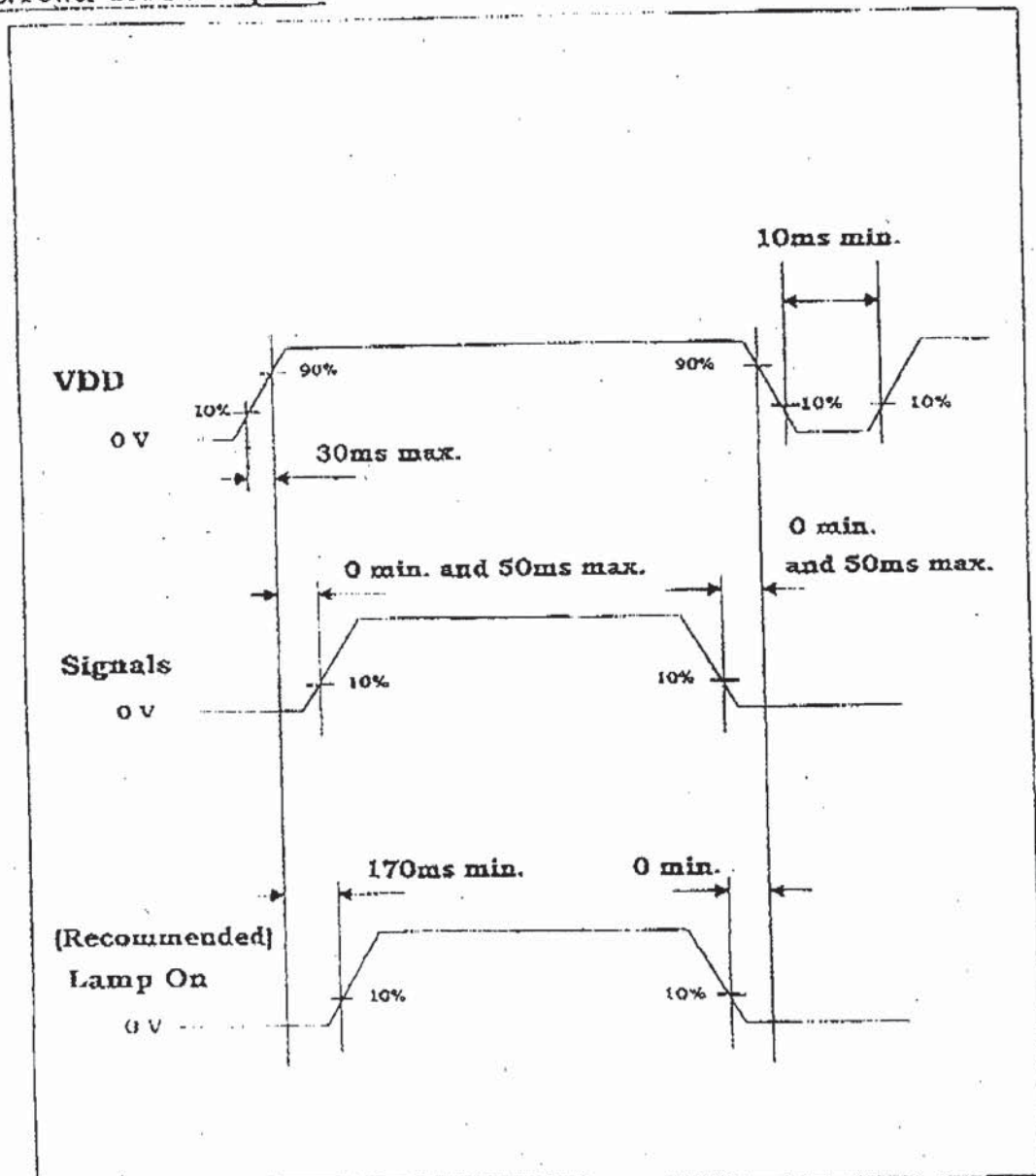
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IBM Customer Acceptance Specifications-ITSV50D2 March 11, 1998**17. Power Requirement**

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit	CONDITION
VDD	Logic/LCD Drive Voltage	+3.0	+3.3	+3.6	V	Load Capacitance 20uF
PDD	VDD Power		0.85		W	VDD=+3.3V
PL	Lamp Power(w/o inverter)		1.5		W	
PDD+PL	Total Power(w/o inverter)		2.35		W	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

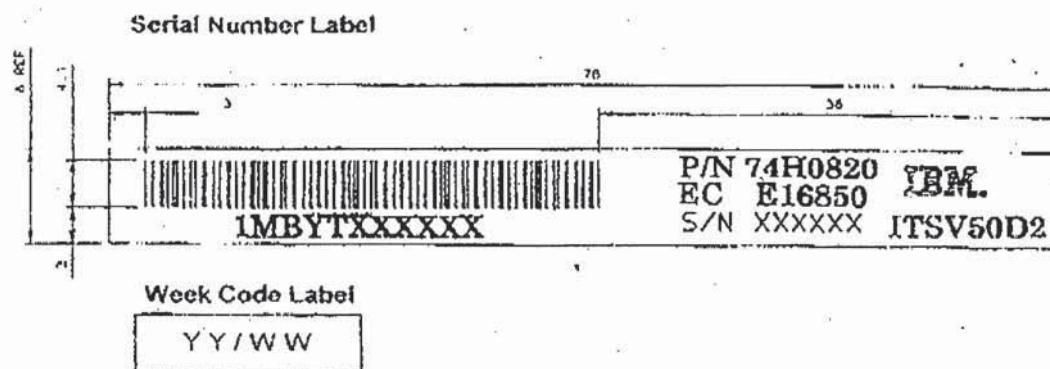
Note: This requirements shall be met with 'All black pattern'.

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IBM Customer Acceptance Specifications-ITSV50D2 March 11, 1998**18. Power ON/OFF sequence**

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19. Product Label



There are two labels at the front limb of the Module Frame.

One is the Serial Number Label and the other is the Week Code Label.

The first 4 digits of the Bar code shows the Module Type **ITSV50D2**

The fifth digit is for the manufacturing location code.

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.

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20. Handling Precautions

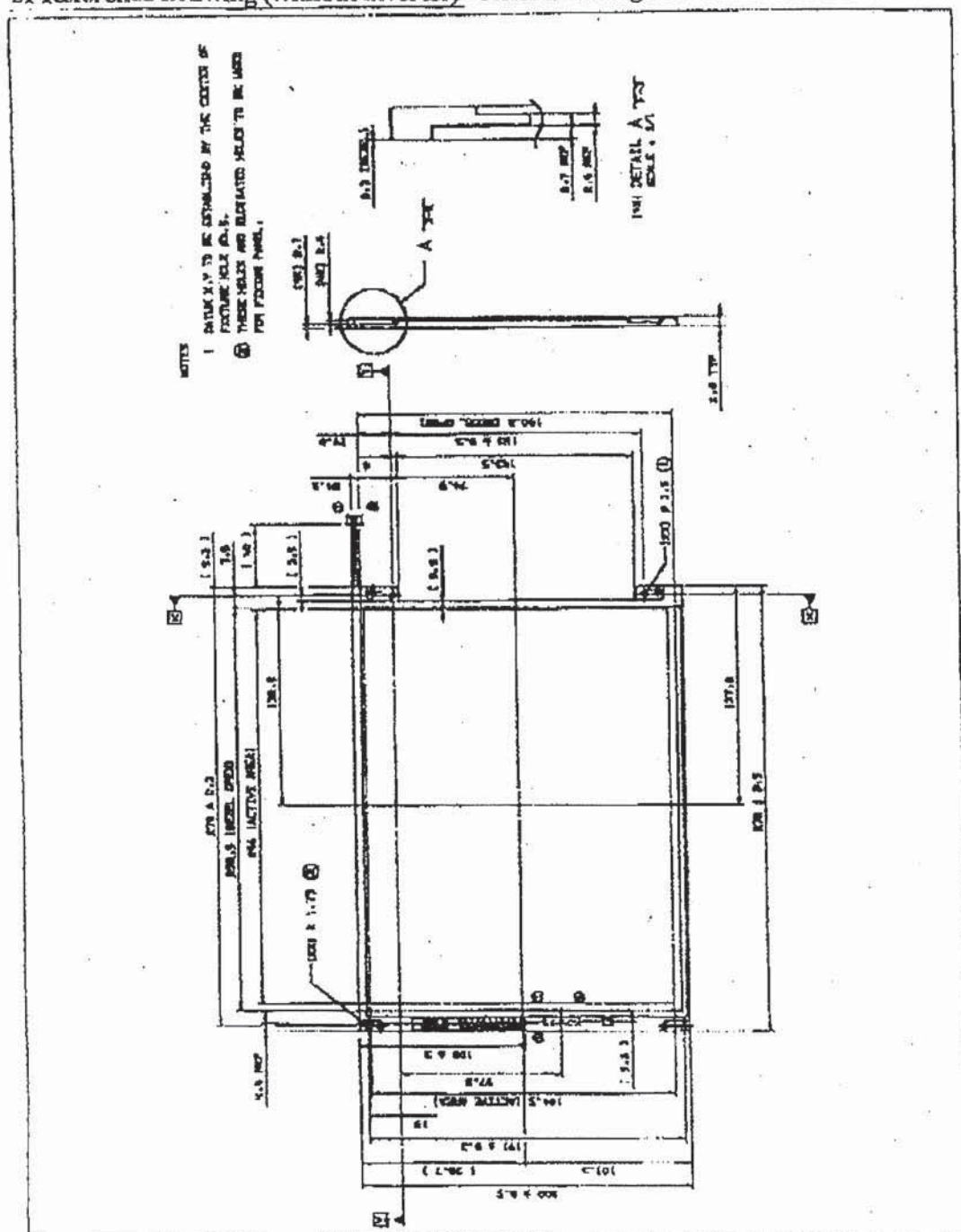
(REFER ALSO THE FIGURES ON NEXT PAGE)

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module. Also be sure to support the metal frame of the TFT Module (by hand, for example) just at the reverse side of the Connector so that the Module itself is not twisted nor bent. Otherwise the TFT Module may be damaged.
- 11) At and after installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.



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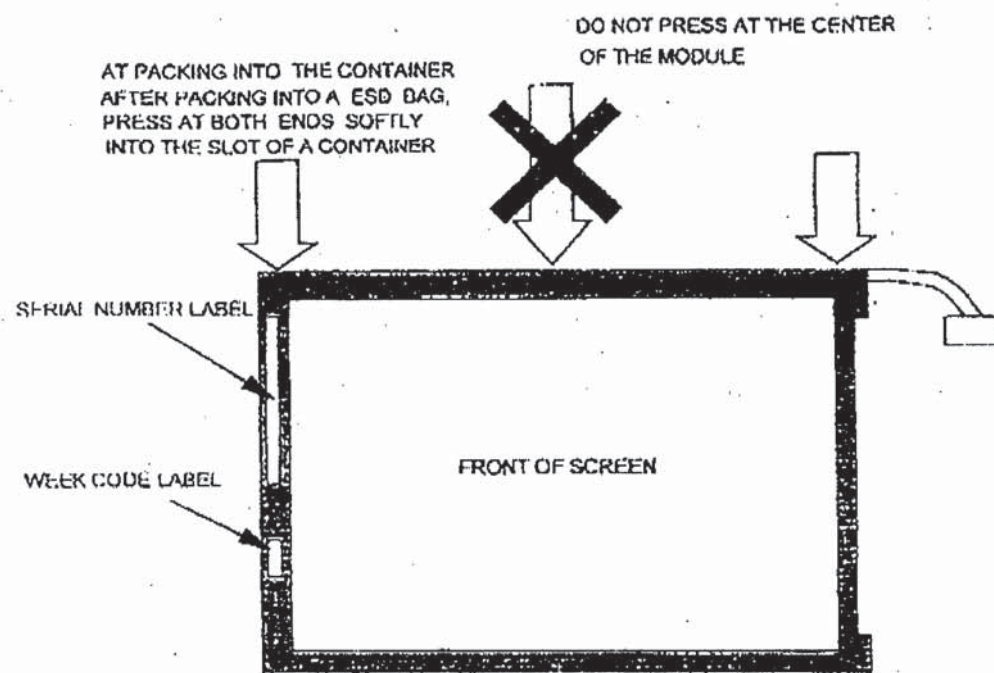
21 Reference Drawing (without inverter) - Refer Drawing P/N 74H0702 for Details



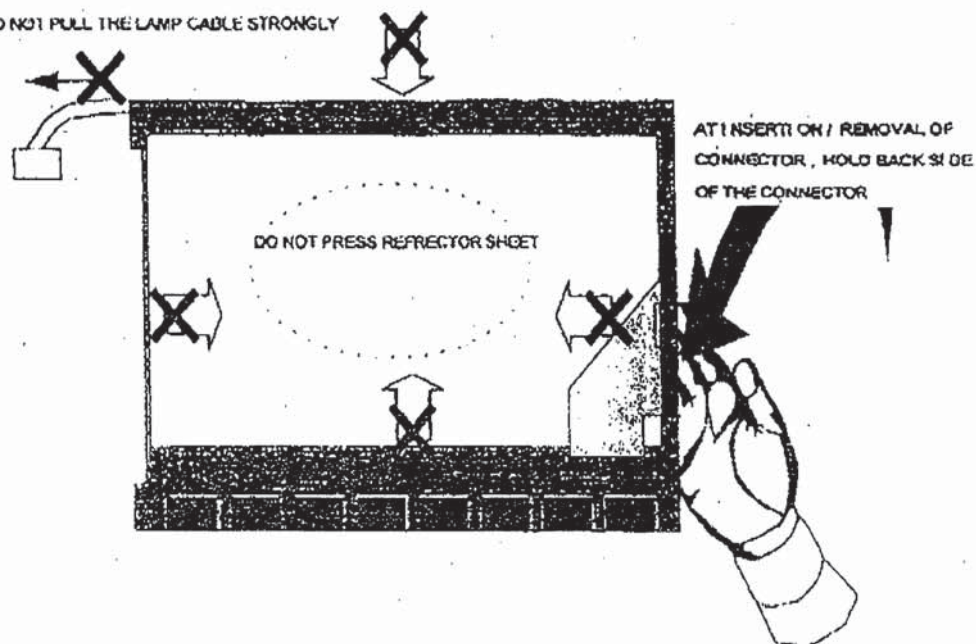
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TOTAL P. 21

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DO NOT PULL THE LAMP CABLE STRONGLY



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